WHAT IS CLAIMED IS:

1. A multiplexer for a biometric apparatus having a signal generator, a sensor, and a processor, the sensor having at least fifty thousand piezo ceramic elements arranged in a two-dimensional array and spaced at a pitch equal to or less than approximately two hundred microns, each of the at least fifty thousand piezo ceramic elements having a first end and a second end, comprising:

a plurality of first conductors coupled to the first ends of piezo ceramic elements in corresponding rows;

a plurality of first switches each of which is coupled to a respective one of said plurality of first conductors;

a plurality of second conductors coupled to the second ends of piezo ceramic elements in corresponding columns; and

a plurality of second switches each of which is coupled to a respective one of said plurality of second conductors,

wherein said plurality of first conductors are approximately orthogonal to said plurality of second conductors, and

wherein said plurality of first switches are controlled to couple a signal output from an output port of the signal generator to a particular piezo ceramic element of the at least fifty thousand piezo ceramic elements, and

wherein said plurality of second switches are controlled to couple a signal associated with the particular piezo ceramic element of the at least fifty thousand piezo ceramic elements to an input port of the processor.

2. The multiplexer of claim 1, wherein each of said plurality of first switches and said plurality of second switches is a three-way switch.

3. The multiplexer of claim 2, wherein each of said plurality of first switches connects one of said plurality of first conductors to one of the input signal generator, a high impedance open node, and a low impedance ground node.

4. The multiplexer of claim 2, wherein each of said plurality of second switches connects one of said plurality of second conductors to one of the processor, a high impedance open node, and a low impedance ground node.

5. The multiplexer of claim 1, further comprising:

at least one shift register, coupled to said plurality of first switches, that controls the position of said plurality of first switches.

6. The multiplexer of claim 5, further comprising:

a controller, coupled to said at least one shift register, that controls the operation of said at least one shift register.

7. The multiplexer of claim 6, further comprising:

at least one shift register, coupled to said plurality of second switches, that controls the position of said plurality of second switches.

8. The multiplexer of claim 7, wherein said controller is coupled to said at least one shift register coupled to said plurality of second switches and controls the operation of said at least one shift register coupled to said plurality of second switches.

9. The multiplexer of claim 1, wherein said plurality of first conductors and said plurality of second conductors are a formed using a vacuum deposition process.

10. The multiplexer of claim 1, wherein said plurality of first conductors and said plurality of second conductors are a formed using a lithography process.

11. The multiplexer of claim 1, wherein said plurality of first switches comprise at least two separate integrated circuit chips.

12. The multiplexer of claim 11, wherein said plurality of second switches comprise at least two separate integrated circuit chips.

13. A multiplexer for a biometric apparatus having a signal generator, a sensor, and a processor, the sensor having at least fifty thousand piezo ceramic elements arranged in a two-dimensional array spaced on a pitch equal to or less than approximately two hundred microns, each of the at least fifty thousand piezo ceramic elements having a first end and a second end, the two-dimensional array having X rows with Y piezo ceramic elements in each of the X rows, comprising:

a plurality of first conductors each of which is coupled to the first end of Y of the at least fifty thousand piezo ceramic elements;

a plurality of second conductors each of which is coupled to the second end of X of the at least fifty thousand piezo ceramic elements;

a plurality of first switches coupled to said plurality of first conductors;

a plurality of second switches coupled to said plurality of second conductors;

at least one shift register, coupled to said plurality of first switches, that controls the position of said plurality of first switches;

at least one shift register, coupled to said plurality of second switches, that controls the position of said plurality of second switches; and

a controller, coupled to said at least one shift register coupled to said plurality of first switches and said at least one shift register coupled to said plurality of second switches, that controls the operation of said at least one shift register coupled to said plurality of first switches and said at least one shift register coupled to said plurality of second switches.

14. The multiplexer of claim 13, wherein each of said plurality of first conductors is approximately orthogonal to each of said plurality of second conductors.

15. The multiplexer of claim 13, wherein said plurality of first switches are controlled to couple an output port of the signal generator to a particular piezo ceramic element of the at least fifty thousand piezo ceramic elements.

16. The multiplexer of claim 15, wherein said plurality of second switches are controlled to couple the particular piezo ceramic element of the at least fifty thousand piezo ceramic elements to an input port of the processor.

17. The multiplexer of claim 13, wherein each of said plurality of first switches and said plurality of second switches is a three-way switch.

18. The multiplexer of claim 17, wherein each of said plurality of first switches connects one of said plurality of first conductors to one of an input port of the signal generator, a high impedance open node, and a low impedance ground node.

19. The multiplexer of claim 18, wherein each of said plurality of second switches connects one of said plurality of second conductors to one of an input port of the processor, a high impedance open node, and a low impedance ground node.

20. The multiplexer of claim 13, wherein each of said plurality of first conductors and said plurality of second conductors has a width of less than two hundred microns.